Homework Assignment 09

**Question 1** A filter has the transfer function shown—at what frequency will it “ring” in response to a step input? Support you claim. (2 points)

\[
H(s) = \frac{s + 20}{s^2 + 8s + 100}
\]

Comparing the denomination with the standard form shows that \( \zeta = 4/\sqrt{100} = 0.4 \). The system will ring at \( 10\left(\sqrt{1 - \zeta^2}\right) = 9.165 \text{ rad/s} = 1.459 \text{ Hz} \).

**Question 2** A filter has the transfer function shown—what type of filter is this (LPF, BPF, etc.) Support you claim. (2 points)

\[
H(s) = \frac{3s + 20}{s^3 + 8s + 100}
\]

This is a 3rd order LPF. Let \( s = j\omega \), then \( H(0) = 20/100 = 5 \), the dc response. As \( \omega \to \infty \), \( H \to 0 \). This is an LPF. Referring to Question 1, we know that \( \zeta = 0.4 \), so there will be peaking at some frequency in the passband.

**Question 3** True or false: For a PLL, the lock (or hold range) is always larger than the capture range. (1 point)

**True**

**Question 4** In some PLL circuits the VCO output is divided by two, even if the PLL is not used as a \( \times 2 \) frequency multiplier. What is the purpose of the division? Hint: consider the requirements for and XOR gate to function as a phase detector.

![Diagram](image)

Dividing by two is an easy way to ensure a 50% duty cycle, which is required for the XOR (low noise) phase detector to work properly.
**Question 5**  A first-order PLL with $K_v = 10^4 \text{ s}^{-1}$ uses a VCO with $K_o = 5 \text{ kHz/V}$ and the VCO has no offset. That is, the output is zero when the VCO input is 0 V. Assume the PLL is locked to a 10-kHz signal. The signal is modulated by a 2.5-kHz sine wave resulting in a $\pm 10\%$ frequency deviation. Determine the VCO control voltage $v_e(t)$. (8 points)

**Solution**  The first step is to draw a diagram with all the pertinent information included. The PLL is locked onto a signal that deviates between 0.9 kHz and 1.1 kHz with an average value of 10 kHz. The 10-kHz average value will result in a dc value of 2 V for $v_e(t)$. Below we focus on the deviation and its rate of deviation, and add the dc value at the end.

To avoid confusion, convert to rad/s throughout. Thus $K_o = 10^4 \pi \text{ rad} \cdot \text{s}^{-1} \cdot \text{V}^{-1}$. The frequency deviation is $f_i(t)$ which has amplitude 1 kHz:

$$f_i(t) = (1 \times 10^3) \cos(2\pi f_m t) \text{ Hz} \Rightarrow \omega_i = 2\pi \times 10^3 \cos(2\pi 2500t) \text{ rad/s}$$

![Diagram of PLL](image)

For 1st order loop

$$\frac{v_e(s)}{\omega_i(s)} = \frac{K_v}{s + K_v} \Rightarrow \frac{v_e(j\omega)}{\omega_i(j\omega)} = \frac{1/\omega_i}{1 + j\omega/K_v}$$

Solve for $v_e(j\omega)$ at $\omega = 2\pi(2500)$ rad/s:

$$\frac{v_e(j\omega)}{\omega_i(s)} = \frac{1/10^4\pi}{1 + j2\pi(2500)/10^4} = 17.6\angle -57.52^\circ \mu\text{V per rad/s}$$

$$\omega_i = 2\pi \times 10^3 \cos(2500t) \text{ rad/s} = 2\pi \times 10^3 \angle 0^\circ \text{ rad/s}$$

$$v_e(j\omega) = (2\pi \times 10^3 \angle 0^\circ)(17.6 \times 10^{-6} \angle -57.52^\circ) \text{ rad/s}$$

$$= 0.1075\angle -57.52^\circ$$

Finally, convert back to the time domain and add the dc value as discussed above:

$$v_e(t) = 2 + 0.1074 \cos(2\pi 2500t - 57.52^\circ) \text{ V}$$
**Question 6** Consider the PLL shown where $K_v = 10^4$ and $K_o = 1$ krad/s per V.

![PLL Diagram]

(a) What is the order of the loop? (1 point)

1$^{st}$ order

(b) Write down an expression for the transfer function $H(s) = \theta_o(s)/\theta_i(s)$. (2 points)

$$H(s) = \frac{10^4}{s + 10^4}$$

(c) Write down an expression for the transfer function $H(s) = V_{VCO}(s)/\omega_i(s)$ (2 points)

$$H(s) = \frac{1}{K_o} \frac{10^4}{s + 10^4} = \frac{10}{s + 10^4}$$

(d) What is the time constant of the loop? (1 point)

$$\tau = 1/K_v = 100 \mu s$$

(e) What is the 3-dB bandwidth of the loop in Hz? (1 point)

$$f_{3dB} = 1/2\pi\tau = 1.6 \text{ kHz}$$

(f) If the input frequency changes with a step, what is the rise time of the VCO control voltage assuming the loop stays in lock? (1 point)

$$t_r \approx 2.2\tau = 220 \mu s \text{ or } t_r \approx 0.35/BW \approx 220 \mu s$$

(g) The loop is locked to a 100-kHz signal. If the input frequency changes with a step to 100.5 kHz. By how much does the control voltage change? (1 point)

$$\frac{(2\pi)(\Delta f)}{K_o} = \frac{(2\pi)(5 \times 10^2)}{1 \times 10^3} = \pi V$$
**Question 7** A second-order PLL has the following parameters

\[ K_o = 1 \text{ kHz/V}, \quad \omega_p = 2.5 \text{ krad/s}, \quad \omega_z = 300 \text{ krad/s}, \quad \omega_n = 5 \text{ krad/s}, \quad \text{and} \quad \zeta = 0.25 \]

Sketch the change in VCO control voltage when the input frequency changes abruptly by 1 kHz. Provide as much details as you can, but you are NOT expected to perform lengthy calculations. Do NOT calculate % overshoot. (4 points)
Question 8  Show that one can use an AND gate as a phase detector, then find the detector constant $K_d$. Be sure to supply the correct units for $K_d$.  Hint: draw square wave $x(t)$ feeding one input of the AND gate and square wave $y(t)$ feeding the other input. Consider the phase detector’s output when $x$ and $y$ are in phase, $y$ lags by 90°, and $y$ lags by 180°.  (5 points)

Let the amplitude for $x$ and $y$ be $V_{CC}$. When the signals are in phase, then the average value of the output is $0.5 V_{CC}$. When the phase difference is 90°, the average value is $0.25 V_{CC}$, and when the phase difference is 180°, then the output is 0. From this and the figure below it is clear that $K_d = 0.5 V_{CC} / \pi$ V/ rad
**Question 9** Write a short poem that expresses your feelings towards PLLs, using rhyming couplets. You have poetic license. *(2 points)*

**Question 10** You are to design a PLL-based FM demodulator. The input is low-quality (small SNR) audio. You have a choice of PDs: Type I, Type II, Type III, etc. Which of the PDs will you use? Explain your answer. *(4 points)*

The best choice would be an analog multiplier, and the second best would be an XOR-gate. The reason is that they exhibit the best performance with respect to noise. For example, the Type II PD responds to the edges of its inputs. This has advantages (i.e., the inputs don’t have to have 50% duty cycle), but it also implies that glitches affect the PD output. The analog/XOR type PDs will also respond to glitches, but their outputs are more related to the overall average, and are less affected by noise.

**Question 11** You are to design a PLL-based detector for demodulating telemetry data that are FSK-encoded. The data come from a transmitter on a spacecraft and the SNR is low. You have a choice of PDs: Type I, Type II, Type III, etc. Which of the PDs will you use? Explain your answer. *(4 points)*

The best choice would be an analog multiplier, and the second best would be an XOR-gate. The reason is that they exhibit the best performance with respect to noise. For example, the Type II PD responds to the edges of its inputs. This has advantages (i.e., the inputs don’t have to have 50% duty cycle), but it also implies that glitches affect the PD output. The analog/XOR type PDs will also respond to glitches, but their outputs are more related to the overall average, and are less affected by noise.

**Question 12** You are to design a PLL-based circuit that lock onto the 60-Hz mains frequency. You have a choice of PDs: Type I, Type II, Type III, etc. Which of the PDs will you use? Explain your answer. *(4 points)*

The best choice would be an analog multiplier, and the second best would be an XOR-gate. The reason is that they exhibit the best performance with respect to noise. For example, the Type II PD responds to the edges of its inputs. This has advantages (i.e., the inputs don’t have to have 50% duty cycle), but it also implies that glitches affect the PD output. The analog/XOR type PDs will also respond to glitches, but their outputs are more related to the overall average, and are less affected by noise. With an analog/XOR PD one can make the PLL bandwidth very small. This is because the input (60 Hz mains) is unlikely to change much. The machines that generate the power are large and have mechanical inertia, and the frequency power companies generate are regulated by law.