Radio Frequency Electronics

Active Components II

- Born in 1889 in Sweden
- Received B.S. and M.S. from U. North Dakota
- Received Ph.D. from Yale
- Worked and Bell Laboratories for all of his career.
- Known for Nyquist rate, Nyquist plots, Nyquist stability criterion, Johnson-Nyquist noise, Nyquist-Shannon Sampling Theorem, and others.
- Died in 1976

Harry Nyquist
With proper doping levels and doping profile, one can make the reverse recovery a very narrow pulse.

From Linear Systems theory we know that narrow pulses have significant harmonics.

This is used in **Step Recovery Diodes** to generate high frequencies.
Step-Recovery Diodes

Example of an SRD

SRD in Housing

3 mm
Comb Generators
SRD Frequency Multiplier

Filters to remove all but the desired harmonics

SRD

Transmission Line

OUTPUT SPECTRUM (dBm)

FREQUENCY (GHz)
Diode parameters in SPICE
### Diode parameters in SPICE

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Value</th>
</tr>
</thead>
<tbody>
<tr>
<td>$C_{J0}$</td>
<td>47.636138775999P</td>
</tr>
<tr>
<td>$I_0$</td>
<td>3.51E-1N</td>
</tr>
<tr>
<td>$R_S$</td>
<td>121.232917696026M</td>
</tr>
</tbody>
</table>

- $V_{BR}$
- $V_{bi}$
Junction gradient coefficient

Energy Bandgap

Diode parameters in SPICE
Amplitude-modulated (AM) signal

Information

RF Carrier

Diode detector

Detected signal

Proper choice of $RC$ constant important

$RC$ too large $\Rightarrow$ output will not change fast enough and output will be distorted

$RC$ should be about 0.5 of carrier frequency
Crystal Sets

http://www.schmarder.com/radios/crystal/
Junction Field Effect (JFET) Transistors
JFETs have characteristics that make them useful in some RF circuits, often at the front end.
Note that the device is inherently symmetrical and in many (but not all) commercial JFETs one can interchange the drain and source.
Increasing reverse-bias at gate increases depletion region that extends into channel, which constricts flow of carriers (electrons) in channel.
Post pinch off

Depletion region is different across channel and channel narrows.

Voltage drop across channel $V_D = 5\, \text{V}$ (and $V_G = 0$)

With large enough $V_D$, channel pinches off. $V_{DS} = V_{Dsat}$

Some current still flows

Small, $V_D$ (and $V_G = 0$)

Equilibrium
Small, $V_D$ (and $V_G = 0$)

Depletion region is different across channel and channel narrows.

With large enough $V_D$, channel pinches off. $V_{DS} = V_{Dsat}$

Some current still flows

$|V_P| =$ pinch-off voltage $= V_{Dsat}$ when $V_G = 0$
At small values of $V_D$ or $V_{DS}$ the plot can be quite linear.

Plots such as these ($I_D$ versus $V_D$ or $V_{DS}$) are called the output characteristics of the device.
In saturation, with fixed $V_G$ the device behaves like a constant current source – current through the device is independent of the voltage across the device.

Compliance voltage the smallest voltage across while it stall behaves as a current source.
JFET as a Constant Current Source

At small load current the device looks like a resistor, but at large load currents the channel pinched off and limits further increase.

Simple short-circuit protection

Here $V_G = 0$ and we are on this part of the curve.

Here $I_D$ generates a voltage drop, so that $V_G < 0$, which widens the depletion region.

Thus, it pinches off at a lower current.
$g_m$ is the transconductance and is tied to the current-source nature of the JFET. Similar to $g_m = 40I_C$ for BJT, but, but $10-20 \times$ smaller…

$g_d$ models the channel conductance and is similar to $r_o$ for the BJT.

$C_{gd}$ and $C_{gs}$ models the junction capacitances.

$C_{gd}$ and $C_{gs}$ are small, few pF.
The JFET model is illustrated with a characteristic curve showing the drain current ($I_D$) as a function of drain voltage ($V_D$) for $V_G = 0$ and $V_G < 0$. The JFET model includes a drain current source $i_d$, a gate voltage $V_G$, a drain voltage $V_D$, and source voltage $V_S$. The figure also shows the mathematical expressions for the drain conductance ($g_d$) and transconductance ($g_m$):

$$g_d = \left. \frac{\partial I_D}{\partial V_D} \right|_{V_G=\text{constant}}$$

...the drain or channel conductance

$$g_m = \left. \frac{\partial I_D}{\partial V_G} \right|_{V_D=\text{constant}}$$

...transconductance or mutual conductance
Plots such as these \((I_D \text{ versus } V_G \text{ or } V_{GS})\) are called the **transfer characteristics** of the device.

\[
I_D = I_{DSS} \left(1 - \frac{V_{GS}}{V_P}\right)^2
\]
Applications of JFETs

- Constant current generators. Used in ICs
- Current limiting devices. Board level and ICs.
- Input stages of amplifier for very high input resistance.
- Pinch resistors.
- Input stages of amplifiers with very low noise.
- Voltage-controllable resistors. Used variable gain amplifiers, automatic gain control AGC, stages, Wien bridge stabilization.
- No diffusion capacitance, so have good high frequency response.
- JFETS make good mixers
### Production Spread

From datasheet for 2N3070

<table>
<thead>
<tr>
<th>PARAMETER</th>
<th>MIN.</th>
<th>TYP</th>
<th>MAX.</th>
<th>UNIT</th>
<th>TEST CONDITIONS</th>
</tr>
</thead>
<tbody>
<tr>
<td>BvGSS</td>
<td>40</td>
<td>55</td>
<td>6</td>
<td>V</td>
<td>V_{DS} = 0, I_G = 1\mu A</td>
</tr>
<tr>
<td>IDSS</td>
<td>0.1</td>
<td></td>
<td>6</td>
<td>mA</td>
<td>V_{DS} = -15V, V_GS = 0</td>
</tr>
<tr>
<td>V_P</td>
<td>0.5</td>
<td></td>
<td>6</td>
<td>V</td>
<td>V_{DS} = -15V, I_D, = 1nA</td>
</tr>
<tr>
<td>I_GSS</td>
<td>20</td>
<td></td>
<td>100</td>
<td>pA</td>
<td>V_{DS} = 0, V_GS = 30V</td>
</tr>
<tr>
<td>G_m</td>
<td>0.2</td>
<td>1</td>
<td>2</td>
<td>mS</td>
<td>V_{DS} = -15V, V_GS = 0, f = 1KHz</td>
</tr>
<tr>
<td>Ciss</td>
<td>4</td>
<td></td>
<td>5</td>
<td>pF</td>
<td>V_{DS} = -15, V_GS = 0, f = 1MHz</td>
</tr>
<tr>
<td>Crss</td>
<td>0.9</td>
<td></td>
<td>1.5</td>
<td>pF</td>
<td>V_{DS} = -15V, V_GS = 0, f = 1MHz</td>
</tr>
</tbody>
</table>

Notice the very large spread in important parameters.

- Notice the comparatively low transconductance.
- BJT @ 1 mA has $g_m$ of about 40 mS
A very common method of biasing a JFET is called *self-biasing* and looks a bit unusual when compared to BJT and MOSFET biasing.

Self biasing consist of forcing the JFET’s gate to 0 V. Since the gate current is very small, one can use large-value resistors, preserving the high input impedance of the JFET.

It is not unusual to see values of several MΩ used.

From a bias perspective, the value of $R_G$ is in most cases non-critical.

\[
I_D = I_{DSS} \left(1 - \frac{V_{GS}}{V_P}\right)^2
\]

\[
V_{GS} = -I_D R_S
\]

\[
-\frac{V_{GS}}{R_s} = I_{DSS} \left(1 - \frac{V_{GS}}{V_P}\right)^2
\]

\[
\text{Combine and solve for } V_{GS}
\]

\[
\text{Load line}
\]

\[
\text{Slope is } -\frac{1}{R_s}
\]

\[
\text{I}_D-V_{GS} \text{ relationship for } n \text{ JFET}
\]

\[
\text{KVL around } R_s, \text{ Gate and } R_g
\]
Assume $I_{DSS} = 10$ mA, and $V_P = -3$ V, find $V_S$ and $I_D$. Check with SPICE.

**Solution**

\[ I_D = I_{DSS} \left( 1 - \frac{V_{GS}}{V_P} \right)^2 \]

\[ V_{GS} = -I_D R_S \]

\[ -\frac{V_{GS}}{4,700} = 0.01 \left( 1 - \frac{V_{GS}}{-3} \right)^2 \]

\[ V_{GS} = -3.856 \text{ V}, \quad V_{GS} = -2.33 \text{ V} \]

\[ I_D = 8.2 \text{ mA}, \quad I_D = 0.497 \text{ mA} \]

\[ V_S = 38.5 \text{ V}, \quad V_S = 2.34 \text{ V} \]

**SPICE Check**

For the JFET set

\[ \text{BETA} = \frac{I_{DSS}/V_P^2}{1.11 \times 10^{-3}} \]

\[ V_{TO} = -3 \]

**SPICE Gives**

\[ I_D = 0.482 \text{ mA} \]

\[ V_S = 2.266 \text{ V} \]
JFET Self Biasing

... works...

... but it is probably better to use a coupling capacitor.
That's All Folks